Amendment s to the Claims:

This listing of the claims will replace all prior versions and listings of the claims in the application:

Listing of the Claims:

1. (Currently amended) In a method for designing a circuit where design parameters for performance specifications are represented by posynomial expressions with constraints and solved with geometric programming, an improvement for simultaneously determining the boundaries for circuit elements in the floorplan of the circuit comprising:

representing the boundaries for circuit elements in the floorplan of the circuit as posynomial expressions with constraints on circuit size;

simultaneously solving the posynomial expressions for the design parameters and solving the posynomial expressions for the floorplan boundaries on a computer using geometric programming; and,

outputting the results of the solving in a format that allows the results to be used to layout the circuit.

2. (Previously presented) The method defined by claim 1 wherein the representation of the floorplan of the circuit includes the slicing of the circuit along the boundaries of the circuit elements.

3. (Previously presented) The method defined by claim 1 including using layout constraints for the floorplan.

4. (Previously presented) The method defined by claim 3 wherein one of said layout constraints is a limitation on the circuit area.

5. (Previously presented) The method defined by claim 4 wherein another of said layout constraints is a limitation on the aspect ratio of the circuit layout.

6. (Previously presented) In a method for designing an analog integrated circuit having active circuit elements where design parameters for performance specifications are represented by posynomial expressions with constraints and then solved with geometric programming, an improvement for simultaneously determining the boundaries for the active circuit elements in a floorplan for the integrated circuit, comprising:

representing the floorplan as posynomial constraints of vertical and horizontal dimensions for regions where the active circuit elements are placed;

simultaneously solving the posynomial expressions for the design parameters and the posynomial constraints for the vertical and horizontal dimensions; and

outputting the results of the solving in a format usable to layout the integrated circuit.

7. (Original) The method defined by claim 6 wherein the integrated circuit is sliced vertically and horizontally along the boundaries of the circuit elements.

8. (Original) The method defined by claim 7 wherein for a vertical slice, the resulting first sibling nodes are represented by a sum of horizontal dimensions of the first sibling nodes being equal to or less than a first parent node and which dimensions of the first sibling nodes each being equal to or less than a vertical dimension of the first parent node.

9. (Original) The method defined by claim 8 wherein for each horizontal slice, the resulting second sibling nodes are represented by the sum of the vertical dimensions of the second sibling nodes being equal to or less than a second parent node, and the horizontal dimensions of second sibling nodes each being equal to or less than a vertical height of the second parent node.

10. (Previously presented) The method defined by claim 9 wherein the circuit elements include MOS transistors where the vertical dimension and horizontal dimension of each of the MOS transistors is represented by a posynomial expression.

11. (Original) The method defined by claim 10 wherein the posynomial expression for the vertical and horizontal dimensions of the MOS transistors include process dependant parameters.

12. (Original) The method defined by claim defined by claim 11 wherein the design of the analog circuit presupposes that the active circuit elements are operating in their saturation regions.

13. (Currently amended) A machine readable medium having stored thereon instructions which when executed by a processor cause the processor to perform in a method for designing a circuit where design parameters for performance specifications are represented by posynomial expressions with constraints and solved with geometric programming and for simultaneously determining the boundaries for circuit elements in the floorplan of the circuit, the method, comprising:

simultaneously solving the posynomial expressions for the design parameters of the circuit and solving posynomial expressions for the floorplan boundaries of the circuit elements using geometric programming, the posynomial expressions for the floorplan boundaries represented as constraints on circuit size; and,

outputting the results of the solving in a format that allows the results to be used to layout the circuit.

14. (Previously presented) The machine readable medium defined by claim 13 wherein the representation of the floorplan of the circuit includes the slicing of the circuit along the boundaries of the circuit elements.

15. (Previously presented) The machine readable medium defined by claim 13 including using layout constraints for the floorplan.

16. (Previously presented) The machine readable medium defined by claim 15 wherein one of said layout constraints is a limitation on the circuit area.

17. (Previously presented) The machine readable medium defined by claim 16 wherein another of said layout constraints is a limitation on the aspect ratio of the circuit layout.

18. (Currently amended) A machine readable medium having stored thereon instructions which when executed by a processor cause the processor to perform a method for designing an analog integrated circuit having active circuit elements where design parameters for performance specifications are represented by posynomial expressions with constraints and then solved with geometric programming, and for simultaneously determining the boundaries for the active circuit elements in a floorplan for the integrated circuit, the method comprising:

representing the floorplan as posynomial constraints of vertical and horizontal dimensions for regions where the active circuit elements are placed;

simultaneously solving the posynomial expressions for the design parameters and the posynomial constraints for the vertical and horizontal dimensions; and,

outputting the results of the solving in a format usable to layout the integrated circuit.

19. (Previously presented) The machine readable medium defined by claim 18 wherein the integrated circuit is sliced vertically and horizontally along the boundaries of the circuit elements.

20. (Previously presented) The machine readable medium defined by claim 19 wherein for a vertical slice, the resulting first sibling nodes are represented by a sum of horizontal dimensions of the first sibling nodes being equal to or less than a first parent node and which dimensions of the first sibling nodes each being equal to or less than a vertical dimension of the first parent node.

21. (Previously presented) The machine readable medium defined by claim 20 wherein for each horizontal slice, the resulting second sibling nodes are represented by the sum of the vertical dimensions of the second sibling nodes being equal to or less than a second parent node, and the horizontal dimensions of second sibling nodes each being equal to or less than a vertical height of the second parent node.

22. (Previously presented) The machine readable medium defined by claim 8 wherein the circuit elements include MOS transistors where the vertical dimension and horizontal dimension of each of the MOS transistors is represented by a posynomial expression.

23. (Previously presented) The machine readable medium defined by claim 22 wherein the posynomial expression for the vertical and horizontal dimensions of the MOS transistors include process dependant parameters.

24. (Previously presented) The machine readable medium defined by claim 23 wherein the design of the analog circuit presupposes that the active circuit elements are operating in their saturation regions.